UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,375	03/12/2004	Vijay K.G. Sindagi	TI-35832	7298

23494 7590 09/24/2007
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

NOTIFICATION DATE	DELIVERY MODE
09/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
uspto@dlemail.itg.ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/799,375	SINDAGI ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 7-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4, 5 and 7-11 have been examined.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5 January 2007 has been entered.

Withdrawn Objections

2. Applicant, via amendment has overcome the rejection of claims 1, 2, 8 and 9. The rejection has been respectfully withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5 and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kling (U.S. Patent No. 6,883,089 B2) in view of Yamada et al. (U.S. Patent No. 6,877,087 B1) herein referred to as Yamada.

5. Regarding claim 1, Kling discloses a pipelined data processor operating in a plurality of pipeline phases (see fig. 1A) including at least an instruction decode pipeline phase (Front End 160; see col. 3, lines 13-16) and an execution pipeline phase (Execute 164; see fig. 1A) capable of predicated instruction execution (Instruction #4; see fig. 2) dependent upon the state of an instruction designated predicate register (P1; see fig. 2) comprising: a data register file including a plurality of read/write, general purpose data registers (register file 168; col. 3, lines 15-23); an instruction decode unit (instructions are decoded, whatever does this is considered to be the decode unit) operative during said instruction decode pipeline phase (see col. 3, lines 13-16) receiving fetched instructions (see fig. 2) and determining the identity of at least one source operand data register (such as R1; see fig. 2 regarding Instruction #4), a destination operand data register (such as R1; see fig. 2 regarding Instruction #4) and one of a plurality of functional units (Such as a units for Branching, ALU and Load/Store; fig 1C; the term "functional unit" is extremely broad and anything that performs a function would be included by the limitation) for execution of each instruction, said instruction decode unit further identifying a predicate register (P1; see fig. 2) responsive to receipt of a predicated instruction (Instruction #4, see fig. 2); a scoreboard bit

corresponding to each data register (stored in Scoreboard 170; see fig. 1C; col. 3, 16-20) capable of serving as a predicate register (see col. 3, lines 18-20), each scoreboard bit connected to said instruction decode unit (each component in a processor is directly or indirectly connected) to be set to a first digital state (not available) upon determining said corresponding data register is a destination for an instruction (when the data register is a destination of an instruction, the register would be unavailable and therefore the scoreboard bit must be set) and connected to said plurality of functional units to be reset to a second digital state opposite to said first digital state (available) upon functional unit write of a result to said corresponding data register (when the instruction is completed, the register becomes available and the scoreboard must be set. If the score is not set, the processor would stall indefinitely); said plurality of functional units operative during an execution pipeline phase (see fig. 2) connected to said instruction decode unit for performing a data processing operation (adding 5 to; see Instruction #4, fig. 2) on at least one source operand (such as R1; see fig. 2) recalled from at least one corresponding instruction (Instruction #4; see fig. 2) designated source data register (R1) and producing a result (Stored back into R1), said functional unit responsive to an instruction not a predicate instruction (such as instruction 2; see fig. 2) to write said result to an instruction designated destination data register (such as R2), and responsive to a predicate instruction (instruction 4; see fig. 2) to write said result to an instruction designated destination data register (R1) if said corresponding predicate data register (P1) has a first state (available) during said execution pipeline phase (if the

predicate is true) regardless of said state of said corresponding scoreboard bit (see col. 5, lines 15-17;

Note that instructions only enter the execution phase after the scoreboard indicates that the predicate is available. Therefore, the scoreboard is not checked during the execution phase.)

and to nullify said instruction and not write said result if said predicate register has a second state opposite to said first state (if the predicate is true) during said execution pipeline phase regardless of said state of said corresponding scoreboard bit (see explanation above regarding writing the result); and each functional unit is further operative responsive to a predicate instruction (such as Instruction #4, see fig. 2) during said instruction decode pipeline phase (all instructions pass though a decode phase) to nullify said predicate instruction of a following execution phase (the instruction will be nullified in the execution phase) if said predicate register has said second state (false) during said instruction decode pipeline phase and said corresponding scoreboard bit has said second state during said instruction decode pipeline phase (it will be nullified no matter the bit).

Kling does not expressly disclose nullifying said predicate instruction by operating at a reduced power state relative to normal instruction operation.

Yamada teaches nullifying instructions by operating at a reduced power state relative to normal instruction operation (see column 5, lines 46-54).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Kling by nullifying instructions by operating at a

reduced power state relative to normal instruction operation, as taught by Yamada, in order to conserve power (see column 5, lines 46-49).

6. Regarding claim 2, Kling discloses the pipelined data processor of claim 1, wherein: said functional unit is further operative to reset said scoreboard bit to said second digital state upon nullification of said instruction designating a corresponding data register as a destination operand data register.

Note that the processor must update the scoreboard in response to nullifying an instruction. If the scoreboard is not updated, the processor could stall indefinitely waiting for operands to become available.

7. Claims 4-6 recite equivalent limitations as claims 1-3 respectively and are therefore anticipated by the method the processor of Kling uses (see above regarding claims 1-3).

8. Regarding claim 7, Kling discloses the method of claim 4 further comprising the steps of: statically scheduling instruction execution via a compiler (compiling code; when machine code is generated, instructions are scheduled to execute in program order; see fig. 2) and scheduling via said compiler a last write (instruction 3; see fig. 3) to a data register (P1; see fig. 2) before a decode phase of a predicate instruction (instruction 4) designating said data register as a predicate register (certainly the

compiler will schedule the instructions [create the program order] prior to the program being run on a processor [where the decode phase occurs]).

9. Regarding claim 8, Kling discloses the pipelined data processor of claim 1.

Kling does not expressly disclose that each functional unit is operable at said reduced power state by not fetching at least one instruction operand and not toggling a corresponding register read port during said following execution phase.

Yamada teaches functional units operable at said reduced power state by not fetching at least one instruction operand (from register 21; see figs 1 and 6) and not toggling a corresponding register read port during said following execution phase (see col. 6, lines 49-59 regarding not reading data to latch 22).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Kling by not fetching at least one instruction operand and not toggling a corresponding register read port, as taught by Yamada, in order to conserve power (see column 6, lines 57-59).

10. Regarding claim 9, Kling discloses the pipelined data processor of claim 1.

Kling does not expressly disclose each functional unit is operable at said reduced power state by not powering said functional unit during said following execution phase.

Yamada teaches functional units operable at said reduced power state by not powering said functional unit during said following execution phase (see col. 8, lines 30-33).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Kling by not powering said functional unit during said following execution phase, as taught by Yamada, in order to conserve power (see col. 9, lines 3-7).

11. Claims 10 and 11 recite equivalent limitations as claims 8 and 9 and are rejected under the same grounds.

12. Regarding claim 12, Kling discloses the pipelined data processor of claim 1.

Kling does not expressly disclose said scoreboard bit corresponding to each data register capable of serving as a predicate register includes an OR gate having a first input receiving a signal from a corresponding functional unit indicating when a write instruction to said corresponding predicate register commits, a second input receiving a signal from said corresponding functional unit indicating said write instruction to said corresponding predicate register nullifies and an output, and a flip-flop having a set input receiving an input from said instruction decode unit indicating when said corresponding predicate register is a destination for said write instruction, a reset input connected to said output of said OR gate and a Q output indicating a state of said scoreboard bit.

Examiner is taking Official Notice that it would have been obvious at the time of the invention for one of ordinary skill in the art to modify said scoreboard bit corresponding to each data register capable of serving as a predicate register to include

an OR gate having a first input receiving a signal from a corresponding functional unit indicating when a write instruction to said corresponding predicate register commits, a second input receiving a signal from said corresponding functional unit indicating said write instruction to said corresponding predicate register nullifies and an output, and a flip-flop having a set input receiving an input from said instruction decode unit indicating when said corresponding predicate register is a destination for said write instruction, a reset input connected to said output of said OR gate and a Q output indicating a state of said scoreboard bit.

All of these components were all very common and well known in the art at the time of the invention. These components are mere functional equivalents to anything else that would perform the same actions (see above regarding claim 1). Using these components in the combined invention of Kling and Yamada would have been functionally equivalent and would have yielded predictable results.

13. Regarding claim 13, Kling discloses the pipelined data processor of claim 1.

Kling does not expressly disclose each of said plurality of functional units includes a compare to zero unit receiving data from said instruction identified predicate register generating a signal when data stored in said instruction identified predicate register is zero, a first AND gate having a first input receiving said output of said compare to zero unit, a second input receiving a signal indicating when said predicated instruction is in said instruction decode pipeline phase, an inverting input receiving said state of said corresponding scoreboard bit and an output, and a second AND gate

having a first input receiving said output of said compare to zero unit, a second input receiving a signal indicating when said predicated instruction is in said execution pipeline phase; each of said plurality of functional units operable to nullify said predicate instruction of a following execution phase by operating at a reduced power state relative to normal instruction operation upon generation of a signal at said output of said first AND gate, and not write said result of said predicate instruction of a current execution phase upon generation of a signal at said output of said second AND gate.

Examiner is taking Official Notice that it would have been obvious at the time of the invention for one of ordinary skill in the art to the pipelined data processor of claim 1 to have each of said plurality of functional units include a compare to zero unit receiving data from said instruction identified predicate register generating a signal when data stored in said instruction identified predicate register is zero, a first AND gate having a first input receiving said output of said compare to zero unit, a second input receiving a signal indicating when said predicated instruction is in said instruction decode pipeline phase, an inverting input receiving said state of said corresponding scoreboard bit and an output, and a second AND gate having a first input receiving said output of said compare to zero unit, a second input receiving a signal indicating when said predicated instruction is in said execution pipeline phase; each of said plurality of functional units operable to nullify said predicate instruction of a following execution phase by operating at a reduced power state relative to normal instruction operation upon generation of a signal at said output of said first AND gate, and not write said result of said predicate

instruction of a current execution phase upon generation of a signal at said output of said second AND gate.

All of these components were all very common and well known in the art at the time of the invention. These components are mere functional equivalents to anything else that would perform the same actions (see above regarding claim 1). Using these components in the combined invention of Kling and Yamada would have been functionally equivalent and would have yielded predictable results.

Response to Arguments

14. Applicant's arguments filed 5 January 2007 have been fully considered but they are not persuasive.

15. Applicant states:

> The OFFICE ACTION thus states that data is unavailable when a register is the destination of a write. However, the OFFICE ACTION fails to point out any part of Kling et al supporting this assertion. Likewise, the OFFICE ACTION states that the register becomes available when the write instruction completes. Again the OFFICE ACTION points out no part of Kling et al as teaching this subject matter. The scoreboard of Kling et al indicates whether the operands and data in a predicate register are available.

Examiner disagrees. Inherently, if an instruction is in a pipeline, the result register is clearly unavailable because the instruction writing to that register is not completed. Also, when the instruction is complete, the register must inherently become available (otherwise the processor would halt and progress could not be made). It is impossible for data to be available if an instruction which is not completed targets that

register (since the data for that register is stale and must be updated). Once the instruction executes, the data is then available. Since data registers must be targeted in any processor and inherently, if a register is targeted, it is unavailable for at least some amount of time, the system of Kling teaches setting the bit in response to a "write of a result to said corresponding data register" (because it is now unavailable).

16. Applicant states:

> The OFFICE ACTION thus states that data is unavailable when a register is the destination of a write. However, the OFFICE ACTION fails to point out any part of Kling et al supporting this assertion. Likewise, the OFFICE ACTION states that the register becomes available when the write instruction completes. Again the OFFICE ACTION points out no part of Kling et al as teaching this subject matter. The scoreboard of Kling et al indicates whether the operands and data in a predicate register are available.

Examiner disagrees. Inherently, if an instruction is in a pipeline, the result register is clearly unavailable because the instruction writing to that register is not completed. Also, when the instruction is complete, the register must inherently become available (otherwise the processor would halt and progress could not be made). It is impossible for data to be available if an instruction which is not completed targets that register (since the data for that register is stale and must be updated). Once the instruction executes, the data is then available. Since data registers must be targeted in any processor and inherently, if a register is targeted, it is unavailable for at least some amount of time, the system of Kling teaches setting the bit in response to a "write of a result to said corresponding data register" (because it is now unavailable).

17. Regarding the argument directed at operating at reduced power, Examiner disagrees. Firstly, obviousness under 35 USC 103 does not require one reference to teach all limitations. In contrast, one feature of a secondary reference can be shown to have been obvious to combine with a first reference. Secondly, if the processor of Kling stalls the pipeline if the scoreboard bit is a second state, then using simple logic, inherently, it must always stall when a more exclusive state occurs (both the scoreboard is a second state and the predicate is a second state). When "C if A and (B or not B)" then inherently, "C if A and B" is inherently true. Thirdly, Yamada teaches shutting off a potion of a processor when it is not used. Since the pipeline stalls in the system of Kling, it would have been obvious to shut off the unused portions of the processor. This combination would have yielded extremely predictable results. Additionally, the system of Yamada determines when to reduce power at run time during the decode stage. Lastly, the claim merely states that the instruction is in a decode stage and not that the determination occurs at that time.

18. Regarding the argument direct to the term "regardless", Examiner disagrees. As stated in the previous Office Action, if the instruction is in the execution pipeline phase, the scoreboard bit is already known and therefore the decision whether or not to nullify the instruction is not based on the scoreboard bit and it made regardless of the scoreboard bit.

19. Regarding the argument directed to the limitation "a scoreboard bit to a second digital state upon nullification of said instruction designating said corresponding data register as a destination operand data register", Examiner disagrees. As stated in the previous Office Action, if a nullified instruction would not update the scoreboard, the processor would stall indefinitely because the scoreboard would not allow any dependent instructions to execute. Therefore, inherently, if any instruction leaves the pipeline (is nullified or completes), it must update the scoreboard. Additionally, Examiner is not arguing that the nullification is inherent, but if a nullification occurs, the scoreboard MUST be updated. Applicant's invention shows this in fig. 5. Nowhere in the specification does it state that the scoreboard bit is not updated in some cases when instructions are nullified.

20. Regarding claim 7, scheduling is done with a compiler which is done prior to execution.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER

JM 9/17/2007